Amendments to the Specification

Please replace paragraph [0004] with the following amended paragraph:

[0004] FIGS. 1 and 2 are cross-sectional diagrams for explaining a conventional self-aligned contact formation process. Referring first to FIG. 1, an isolation insulating film 1110 is formed in a semiconductor substrate 100 to define a device formation region. A gate 1120 is formed on the semiconductor substrate 100. The gate 1120 includes a gate dielectric film (not shown), a gate conductive film 1123 and 1125, a mask insulating film 1127 and sidewall spacers 1129. ~~A gate dielectric film (not shown), gate conductive films 1123 and 1125, and a mask insulating film 1127 are formed in the device formation region, and an insulating film spacer 1129 is formed at the sidewalls of the gate conductive films 1123 and 1125 and the mask insulating film 1127 to define a gate 1120.~~ A source region 1105a and a drain region 1105b are formed at respective sides of the gate 1120. ~~After an etch stop 1140 is formed~~ An etch stop 1140 is formed on the resultant structure of the semiconductor substrate 100, a first interlayer insulating film 1150 is formed on the etch stop 1140, and a self-aligned contact hole 1160a is formed in the first interlayer insulating film 1150 through a predetermined patterning process.

Please replace paragraph [0016] with the following amended paragraph:

[0016] A photoresist (not shown) is formed ~~in~~ on the mask insulating film 127~~, and a gate pattern is formed in the photoresist by using known alignment exposure processes~~. The mask insulating film 127 is etched to form a hard mask 127 by dry etching in which the patterned photoresist is used as a mask. After the photoresist mask is removed, ~~the gate pattern is transferred to~~ the gate conductive films 123 and 125 are etched by dry etching using the hard mask 127 as ~~an etching~~ a mask. Then, a gate 120 is formed by forming an insulating film spacer 129 made of a silicon nitride

film at the sidewalls of the hard mask 127 and the gate conductive films 123 and 125. Hereinafter, the hard mask 127 is denoted by the same reference numeral as the mask insulating film.

Please replace paragraph [0017] with the following amended paragraph:

[0017] A source region 105a and a drain region 105b are formed on the semiconductor substrate 100 at both sides of the gate 120 by ion implantation in which the gate 120 is used as a mask. Here, a lower oxide film (not shown) may be formed ~~in~~ on the source region 105a and the drain region 105b of the device formation region. The lower oxide film may be formed by thermal oxidation or may be the gate dielectric film 121 remaining in the device formation region.

Please replace paragraph [0019] with the following amended paragraph:

[0019] Still referring to FIG. 3, a first interlayer insulating film 150 is thickly formed on the whole surface of the semiconductor substrate 100, and its surface is planarized by a known planarization process. If the hard mask 127a and the insulating film spacer 129 are nitride films in order to perform a self-aligned contact formation process, it is desirable that the first interlayer insulating film 150 be a silicon oxide film formed by chemical vapor deposition (CVD) so that the first interlayer insulating film 150 can have a high etching selectivity with respect to the hard mask 127 and the insulating film spacer 129 as the silicon nitride films. In particular, it is desirable that the first interlayer insulating film 150 be a silicon oxide film formed by high-density plasma chemical vapor deposition (HDP CVD) because the deposition is executed rapidly, and the ~~capability to fill the pattern~~ step coverage is superior. When the etch stop 140 and the buffer layer 130 are removed by wet etching, the first interlayer insulating film 150 formed by HDP CVD is etched much

slower than the etch stop 140 and the buffer layer 130 by an etchant solution. Thus, damage to a contact pattern by wet etching can be reduced.

Please replace paragraph [0022] with the following amended paragraph:

[0022] Referring to FIG. 4, a photoresist pattern (not shown) is formed on the planarized first interlayer insulating film 150 ~~the first interlayer insulating film 150 that is planarized is covered with a photoresist (not shown), and a self-aligned contact pattern is formed on the photoresist by alignment exposure. Here, the self-aligned contact pattern is formed to connect the source region 105a with the drain region 105b~~. The self-aligned contact hole 160a is formed by etching the first interlayer insulating film 150 by dry etching in which the ~~patterned~~ photoresist pattern is used as a mask. The line width of the self-aligned contact hole 160a is larger than the source region 105a or the drain region 106b. Here, an upper portion of the etch stop 140 serves as an etching stopping boundary, and thus etching of the self-aligned contact hole 160a is stopped on the etch stop 140. Then, the insulating film spacer 129 partially serves as a mask, and thus the self-aligned contact hole 160a is formed at sides of the insulating film spacer 129.

Please replace paragraph [0025] with the following amended paragraph:

[0025] Referring to FIGS. 6 through 8, the buffer layer 130 is removed by wet etching to expose the semiconductor substrate 100 of the source region 105a and the drain region 105b (step S3). Here, an etching solution is used to etch the silicon oxide film buffer layer and is an ammonium hydroxide (NH_4OH) solution at a temperature of 30°C to 80°C. Thus, an etching rate of the silicon oxide film increases, and the time required by the entire process can be greatly reduced since the hot etching solution is used. While an etching process is in progress, the first interlayer insulating film 150, which is a silicon oxide film formed by HDP CVD, is also etched. However,

an etching rate of the first interlayer insulating film 150 is about 2Å per minute. Since the etching rate of the first interlayer insulating film 150 is slower than that of the buffer layer 130 as the etching rates of a mid-temperature oxide (MTO) film, the first interlayer insulating film 150 is not etched or partially etched ~~the buffer layers 130, and the first interlayer insulating film 150 are about 5□ and hundreds of □ respectively while thousands of □ of the first interlayer insulating film 150 is etched per minute~~. Therefore, this wet etching hardly causes damage to the contact hole morphology considering changes in sizes of the contact hole.